Amendments to the Specification:

Please replace the paragraph at page 9, lines 15-20 with the following amended paragraph:

FIG. 3 is a timing diagram showing a write operation of the conventional semiconductor device (in the case of tWR=2 clocks). In general, as shown in FIG. 3, when an activation command signal ACT and an external address signal ~~ADDR~~RA are input at C2 of the master clock signal CLK, the master clock signal CLK having intervals C1-C10, the semiconductor device sets to be activated and the word line signal WL corresponding to the external address signal is activated. The word line signal WL is deactivated by the pre-charge command signal PRE.

Please replace the paragraph at page 9, lines 21-25 with the following amended paragraph:

When a write command signal WRITE and the external address signal ~~ADDR~~CA are input at C4 of the master clock signal CLK, the column address signal CAi (Y0) into which first data D0 are written is activated. When the write command signal WRITE is input, the write enable signal PWR is activated, and accordingly the column address set signal CASET is activated.

Please replace the paragraph at page 10, lines 4-6 with the following amended paragraph:

After column address signal CAi (Y0) into which the first data DO is written is activated, next column address signals Y1, Y2 and Y3 into which the next data D1, D2 and D3 are written are activated by the column address burst counter output signals CNT0, CNT1 and CNT2.

Please replace the paragraph at page 10, lines 10-13 with the following amended paragraph:

The column selection line enable signal PCSLE and the column selection line disable signal PCSLD are activated by the write enable signal PWR, and the column selection line signal

CSL is activated by the column selection line enable signal PCSLE and is deactivated by the column selection line disable signal PCSLD generating column selection line signals CSL0, CSL1, CSL2 and CSL3.

Please replace the paragraph at page 11, lines 25-28 with the following amended paragraph:

As shown in FIG. 5, the column selection line disable signal PCSLD is generated by an AND operation of an AND gate 13 with respect to the master clock signal CLK via a buffer 12 after a predetermined delay time and the write enable signal PWR via a transmission gate 14 activated both by the master clock signal CLK and an inverted signal of the master clock signal CLK inverted by inverter 15.

Please replace the paragraph at page 12, lines 20-25 with the following amended paragraph:

FIG. 7 is a circuit diagram illustrating a column address buffer in a semiconductor device according to an embodiment of the present invention. As shown in FIG. 7, the column address buffer 40, which is reset by the stop signal CNTSTOP of the column address burst counter via an NMOS transistor 42 and is activated by the column address set signal CASET via a transmission gate 41, generates the column address signal CAi as the external address signal ADDR is trasferred via a buffer 43 after a predetermined delay time. The column address set signal CASET inverted by inverter 44 is input to transmission gate 41.

Please replace the paragraph at page 12, line 26 through page 13, line 2 with the following amended paragraph:

After the column address buffer 40 generates the column address signal CAi by means of the external address signal ADDR, it is activated by a signal derived from and AND operation of an AND gate 47 with respect to the master clock signal CLK and an inverted signal of the column address signal CASET via a transmission gate 45 and generates the column address signal CAi as the internal column address signal PCAi is transferred. The signal derived from

and AND operation of an AND gate 47 is inverted by inverter 46 and connected to transmission gate 45.

Please replace the paragraph at page 13, lines 9-17 with the following amended paragraph:

As shown in FIG. 8, the main decoder 60 includes a first PMOS transistor 63 into which a signal derived from an AND operation of an AND gate 61 with respect to the column selection line enable signal PCSLE and the column address selection signal DCAij is input, an NMOS transistor 65 into which the signal derived from the AND operation of the AND gate 61 with respect to the column selection line enable signal PCSLE and the column address selection signal DCAij is input, a second PMOS transistor 64 connected between the first PMOS transistor 63 and the NMOS transistor 65 and into which an inverted signal of the column selection line disable signal PCSLD inverted by inverter 62 is input, and an inverter 66 connected to a point between the second PMOS transistor 64 and the NMOS transistor 65.

Please replace the paragraph at page 14, lines 23-26 with the following amended paragraph:

As shown in FIG. 9, the column address set signal CASET generator 70 generates the column address set signal CASET through an AND operation of an AND gate 74 with respect to the write enable signal PWR and an output signal from the three inverters 71, 72 and 73 in series (a chain of inverters) into which the write enable signal PWR is input and inverted column address set signal CASETB is gnerated by inverting the column address set signal CASET by inverter 75.

Please replace the paragraph at page 15, lines 8-13 with the following amended paragraph:

FIG. 10 is a circuit diagram illustrating a counter controller in a semiconductor device according to an embodiment of the present invention. As shown in FIG. 10, the counter controller 200 generates the stop signal CNTSTOP of the column address burst counter through an AND operation of an AND gate 205 with respect to the third column address burst counter

output signal CNT2 and a corresponding write recovery time (tWR) enable signal ~~tWR1~~PtWR1 in the case that the write recovery time (tWR) is 1 (one clock).

Please replace the paragraph at page 15, lines 14-24 with the following amended paragraph:

The counter controller 200 generates the stop signal CNTSTOP of the column address burst counter through an AND operation of an AND gate 202 with respect to a signal derived from an AND operation of an AND gate 201 with respect to the first column address burst counter output signal CNT0 and the third column address burst counter output signal CNT2 and a corresponding write recovery time enable signal ~~tWR2~~PtWR2 in the case that the write recovery time (tWR) is 2 (two clocks), and generates the stop signal CNTSTOP of the column address burst counter through an AND operation of an AND gate 204 with respect to a signal derived from an AND operation of an AND gate 203 with respect to the second column address burst counter output signal CNT1 and the third column address burst counter output signal CNT2 and a corresponding write recovery time enable signal ~~tWR3~~PtWR3 in the case that the write recovery time (tWR) is 3 (three clocks). The outputs of the AND gates 201, 204 and 205 are connected by an OR gate 206 which outputs the stop signal CNTSTOP.

Please replace the paragraph at page 16, line 18 through page 17, line 1 with the following amended paragraph:

In a similar way, in the counter controller 200, a fourth column address burst counter output signal is generated with a delay by one clock of the master clock CLK, compared to the third column address burst counter output signal CNT2, and has two times a generation period of the third column address burst counter output signal CNT2. Also, the stop signal CNTSTOP of the column address burst counter is generated through an AND operation of an AND gate with respect to a signal derived from an AND operation of an AND gate with the fourth column address burst counter output signal and the third column address burst counter output signal CNT2, and a corresponding write address time enable signal ~~tWR4~~PtWR4. Accordingly, in the case that the write recovery time (tWR) is 4 (four clocks), a generation time of the stop signal

CNTSTOP of the column address burst counter can be delayed by one clock of the master clock signal CLK, compared to the case that the write recovery time (tWR) is 3 (three clocks).

Please replace the paragraph at page 17, lines 10-16 with the following amended paragraph:

As shown in FIG. 11, the write recovery time enable signal 300 includes a PMOS transistor 302 into which an inverted signal of a write recovery time determination signal POWER_UP, inverted by inverter 301, is input, an NMOS transistor 304 into which the inverted signal of a write recovery time determination signal POWER_UP is input, a fuse 303 connected between the PMOS transistor 302 and the NMOS transistor 304 for electrically isolating the NMOS transistor 302 from the NMOS transistor 304 if necessary, and an inverter 305 connected to a point between the fuse 303 and the NMOS transistor 304.

Please replace the paragraph at page 18, line 25 through page 19, line 3 with the following amended paragraph:

FIG. 12 is a timing diagram showing a write operation of a semiconductor device (in the case of tWR=2 clocks) according to an embodiment of the present invention. As shown in FIG. 12, when the activation command signal ACT and the external address signal ~~ADDR~~RA are input at C2 of the master clock signal CLK, the master clock signal CLK having intervals C1-C10, the semiconductor device according to the embodiment of the present invention sets to be activated and the word line signal WL corresponding to the external address signal is activated. The word line signal WL is deactivated by the pre-charge command signal PRE.

Please replace the paragraph at page 19, lines 4-8 with the following amended paragraph:

When the write command signal WRITE and the external address signal ~~ADDR~~CA are input at C4 of the master clock signal CLK, the column address signal CAi into which first data are written is activated. When the write command signal WRITE is input, the write enable signal PWR is activated, and accordingly the column address set signal CASET is activated.